

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Satwant Singh; Cyrus Tsui
Assignee: Lattice Semiconductor Corporation
Title: Delay-Matches ASIC Conversion Of A Programmable Logic Devices
Serial No.: 10/660,814 Filing Date: 09/12/2003
Examiner: Unassigned Group Art Unit: 2819
Docket No.: M-15198 US

Irvine, California
February 3, 2004

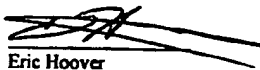
Attn: Official Draftsperson
COMMISSIONER FOR PATENTS
Alexandria, VA 22313-1450

SUBMISSION OF FORMAL DRAWINGS

Dear Sir:

Applicants submit five (5) sheets of formal drawings, consisting of Figures 1, 2, 3, 4a, 4b, 5, 6, and 7, in the above-named application. If there are any questions regarding these drawings, please call the undersigned at (949) 752-7040.

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450, on February 3, 2004.


Eric Hoover

February 3, 2004

Respectfully submitted,



Jon W. Hallman
Attorney for Applicants
Reg. No. 42,622

LAW OFFICES OF
STEPHEN KWOK CHEN
& HEID LLP

2402 MICHELSON DRIVE
SUITE 210
IRVINE, CA 92612
(949) 752-7040
FAX (949) 752-7049